

Claims

- [c1] A barrier stack comprising:
 - a first barrier layer, the first barrier layer comprises a conductive barrier layer; and
 - a second barrier layer above the first barrier layer, the second barrier layer comprises a conductive oxide to enhance the barrier properties of the barrier stack.
- [c2] The barrier stack of claim 1 serves as a barrier for capacitor over plug structure of a memory cell.
- [c3] The barrier stack of claim 2 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.
- [c4] The barrier stack of claim 2 further comprises a plurality of memory cells arranged in a series architecture.
- [c5] The barrier stack of claim 4 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.
- [c6] The barrier stack of claim 1 serves as a barrier for capacitor over plug structure of a ferroelectric memory cell.

- [c7] The barrier stack of claim 6 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.
- [c8] The barrier stack of claim 6 further comprises a plurality of memory cells arranged in a series architecture.
- [c9] The barrier stack of claim 8 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.
- [c10] The barrier stack of claim 1 wherein the first barrier layer comprises first and second conductive sub-barrier layers, wherein an RTO is performed between the formation of the first and second sub-barrier layers.
- [c11] The barrier stack of claim 10 wherein the sub-barrier layers comprises Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c12] The barrier stack of claim 11 wherein the second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c13] The barrier stack of claim 10 wherein the second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c14] The barrier stack of claim 10 wherein an RTO is per-

formed after the first barrier layer is formed and before the second barrier layer is formed.

- [c15] The barrier stack of claim 14 wherein the sub-barrier layers comprises Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c16] The barrier stack of claim 15 wherein the second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c17] The barrier stack of claim 14 wherein the second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c18] The barrier stack of claim 1 wherein an RTO is performed after the first barrier layer is formed and before the second barrier layer is formed.
- [c19] The barrier stack of claim 18 wherein the first barrier layers comprises Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c20] The barrier stack of claim 19 wherein the second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof.
- [c21] The barrier stack of claim 18 wherein the second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof.

nation thereof.

[c22] A method for forming a capacitor over plug structure comprising:
providing a substrate on which an ILD layer is formed and a plug formed on the ILD;
forming a barrier stack over the ILD in contact with the plug, the barrier stack includes first and second barrier layers, the first barrier layer comprises a conductive barrier layer and the second barrier layer above the first barrier layer comprises a conductive oxide to enhance the barrier properties of the barrier stack; and
forming a capacitor over the barrier layer.